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EXAMINER
DINH, TUAN T

ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/681,254	**Applicant(s)** YOON, KI-MYUNG	
	Examiner Tuan T. Dinh	**Art Unit** 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2008*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-24* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☒ All b)☐ Some * c)☐ None of:
1.☒ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 6-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 6, lines 3-4, it is unclear. The phrase of "the backside surface of the semiconductor chip is recessed below a plane defined by the upper surface of the conductive layer" is not understood. As shown in figure 3 of the invention, the insulation substrate (205) having recess for a chip (220) formed on. So, the backside of the semiconductor chip (220) does not have a recess. Please, clarify.

Regarding claim 11, lines 4-5 is unclear. The phrase of "an insulating layer formed on an upper surface of the conductive layer" is not understood, since as shown in the drawings, the insulating layer formed on a **lower surface** of the conductive layer. Please, correct.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 9-13, and 15-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Taniguchi et al. (U.S. Patent 6,489,676), specific on figure 12.

As to claim 1, Taniguchi et al. discloses a multi-chip semiconductor package (20f) comprising:

a plurality of stacked semiconductor package structures (IC stacked structures 20), each semiconductor package structure including;

a substrate (2, in figure 12) having upper and lower surfaces;

a semiconductor chip (4) mounted on the upper surface of the substrate (2), the semiconductor chip including an active surface (the active surface is located on top for wire bond connected to bond pad 12) and a backside surface (the back surface connected on element 5);

an enclosure body (8) covering substantially the entire upper surface of the substrate;

a plurality of conductive studs (18) extending through the enclosure body outside a periphery of the semiconductor chip (4), the conductive studs having upper and lower surfaces; and

at least one conductive member (pad 12 and solder ball 16) formed in contact with the lower surface of at least one of the conductive studs.

As to claim 12, Taniguchi et al. discloses a multi-chip semiconductor package (20f) as shown in figure 12 comprising: upper and lower semiconductor package structures (20), each semiconductor package structure including; a substrate including a conductive layer (5) and an insulating layer (2); a semiconductor chip (4) mounted on the upper surface of the substrate, the semiconductor chip (4) including an active surface and a backside surface; an enclosure body (8) covering substantially the entire upper surface of the substrate; a plurality of conductive studs (18) extending through the enclosure body outside a periphery of the semiconductor chip (4), the conductive studs having an upper surface and a lower surface; wherein at least one conductive member (12, 16) is formed in contact with the lower surface of at least one of the conductive studs (18) of the upper semiconductor package structure (20); and the upper and lower semiconductor package structures are positioned so that the at least one conductive member is in electrical contact with the upper surface of at least one conductive stud (18) of the lower semiconductor package structure (20).

As to claims 2-3, Taniguchi et al. discloses the stacked semiconductor package structures including upper and lower package structures (20, see figure 12) and, the upper package structure and the lower package structure having substantially the same configuration; wherein the at least one conductive member of the upper package structure is in **or** in direct electrical contact with at least one conductive stud of the lower package structure.

As to claims 4-5, Taniguchi et al. discloses the substrate includes a conductive layer (5) and an insulating layer (2) formed on the lower surface on the conductive layer, the active surface of the semiconductor chip (4) includes conductive pads (the pad formed on top surface of the component 4 where the wire bonded 14 connected to) electrically connected to the conductive layer (5).

As to claims 9-10, Taniguchi et al. discloses the at least one conductive member (12, 16) includes a conductive pattern or solder balls (16).

As to claim 11, Taniguchi et al. discloses the substrate includes conductive layer (5) formed on an insulating layer (2); and further wherein a second plurality of conductive studs (18, see figure 12) extend through the insulating layer and are electrically connected to corresponding ones of the plurality of conductive studs (18) extending through the enclosure body (8).

As to claim 13, Taniguchi et al. discloses the at least one conductive member includes a plurality of solder balls (16) electrically connected to the upper and lower of the studs (18) of the upper and lower packages (20).

As to claim 15, Taniguchi et al. discloses the insulating layer includes a resin material (see column 1, lines 38-39) and the conductive layer includes a metallic material (metal).

Regarding claims 16-24, Taniguchi et al. discloses all of the structure of the product claims (claims 1-5, 9-13, and 15), and the method of forming the device is not germane to the issue of patentability of the device itself.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-8, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi et al. in view of Isaak (in the record).

As to claims 6-7, 14, Taniguchi discloses all of the limitations of the claimed invention except for the semiconductor chip mounted on a recess of the substrate and the active surface is substantially coplanar with the plane. Isaak discloses the backside surface of the semiconductor chip (26) mounted on a recessed below a plane defined by the upper surface of the conductive layer (32), and the active surface of the semiconductor chip (26) is substantially coplanar with or recessed below the plane defined by the upper surface of the conductive layer.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Isaak employed in the package of Taniguchi et al. in order to minimum size of the package.

Regarding claim 8, Taniguchi et al. do not specific disclose solder balls formed on the pads of the active surface of the chip. In figure 10, Isaak shows the solder balls formed on the pads of the chip (26) and electrically connected to the conductive layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Issak (figure 10) employed in the package of

Taniguchi et al. in order to perform BGA type package and to minimize size of the package.

Response to Arguments

5. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Farnworth et al., Shim, Kurita, and Nakao disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reichard Dean can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T Dinh/
Primary Examiner, Art Unit 2841.